I CLAIM

1. Apparatus for processing data under control of a computer program, said apparatus comprising:

(i) a processing unit responsive to native program instruction words to perform data processing operations;

(ii) an instruction interpreter responsive to one or more interpreted instruction words specifying a data processing operation to execute native instruction words upon said processing unit to perform said data processing operation; and

(iii) a memory for storing said computer program; wherein

(iv) said computer program includes both native instruction words and interpreted instruction words;

(v) a native code portion invokes interpretation of an interpreted code portion by executing a native code call instruction to said instruction interpreter;

(vi) execution of said native code call instruction triggers generation of a return address specifying a location within said memory for said native code call instruction; and

(vii) said instruction interpreter uses said return address as a pointer to said interpreted code portion within said memory.

2. Apparatus as claimed in claim 1, wherein said return address is an address immediately succeeding an address of said native code call instruction within said memory.

3. Apparatus as claimed in claim 1, wherein said instruction interpreter writes a new value of said return address for use by a native code return instruction as a pointer to a next native code instruction to be executed when interpretation of said interpreted code portion is finished and return is being made to execution of said next native code portion of said computer program.

4. Apparatus as claimed in claim 3, wherein said interpreted code portion finishes with an interpreted return instruction that returns execution to a native code portion at an address pointed to by said return address.

5. Apparatus as claimed in claim 1, wherein said interpreted code portion finishes with an interpreted exit instruction that results in execution of a next native code portion stored within said memory at an address immediately following said exit instruction without a return being made corresponding to said native code call instruction.

6. Apparatus as claimed in claim 1, wherein said processing unit includes a bank of data processing registers and said return address is stored within a predetermined data processing register within said bank of data processing registers upon execution of said native code call instruction.

7. Apparatus as claimed in claim 6, wherein said memory includes a stack memory region and said return address is copied from said predetermined data processing register to said stack memory region upon invocation of said interpreted code portion.

8. Apparatus as claimed in claim 1, wherein substantially each interpreted code instruction word corresponds to a native code instruction word.

9. Apparatus as claimed in claim 8, wherein said native code instruction words form a native code instruction set and said interpreted code instruction words form an interpreted code instruction set, data processing operations provided by said interpreted code instruction set being a subset of data processing operations provided by said native code instruction set.

10. Apparatus as claimed in claim 1, wherein said native code instruction words are X-bit instruction words and said interpreted code instruction words are Y-bit instruction words, X being greater than Y.

11. Apparatus as claimed in claim 1, wherein said native code instruction words specify N-bit data processing operations to be performed by said processing unit and said interpreted code instruction words specify N-bit data processing operations to be performed by said processing unit.

12. Apparatus as claimed in claim 10, wherein said native code instruction words specify N-bit data processing operations to be performed by said processing unit and said interpreted code instruction words specify N-bit data processing operations to be performed by said processing unit and X is equal to N.

13. Apparatus as claimed in claim 12, wherein Y is N/4.

14. Apparatus as claimed in claim 1, wherein said instruction interpreter is a software interpreter provided by an interpreter computer program formed of native code instruction words executed by said processing unit.

15. Apparatus as claimed in claim 14, comprising a cache memory and wherein said software interpreter is, in use, stored within said cache memory.

16. Apparatus as claimed in claim 15, wherein said software interpreter is stored within said cache memory both when executing native program instruction words and interpreted program instruction words.

17. Apparatus as claimed in claim 1, wherein portions of said computer program having less than a threshold required execution speed are provided as interpreted code

instructions words and portions of said computer program having greater than said threshold required execution speed are provided as native code instructions words.

18. Apparatus as claimed in claim 1, wherein portions of said computer program having less than a threshold execution frequency are provided as interpreted code instructions words and portions of said computer program having greater than said threshold execution frequency are provided as native code instructions words.

19. A method of processing data under control of a computer program, said method comprising the steps of:

(i) in response to native program instruction words, performing data processing operations with a processing unit;

(ii) in response to one or more interpreted instruction words specifying a data processing operation, executing with an instruction interpreter native instruction words upon said processing unit to perform said data processing operation; and

(iii) storing said computer program in a memory; wherein

(iv) said computer program includes at least one native code portion and at least one interpreted code portion;

(v) a native code portion invokes interpretation of an interpreted code portion by executing a native code call instruction to said instruction interpreter;

(vi) execution of said native code call instruction triggers generation of a return address specifying a location within said memory for said native code call instruction; and

(vii) said instruction interpreter uses said return address as a pointer to said interpreted code portion within said memory.